Front End Electronics for the CDF-II Time-of-Flight System

C. Chen, M. Jones, W. Kononenko, J. Kroll, G. M. Mayers, F. M. Newcomer, R. G. C. Oldeman, D. Usynin, R. Van Berg

Abstract— **A Time-of-Flight detector (TOF) has been added to the CDF-II experiment to provide charged kaon identification primarily for neutral B meson flavor determination. The TOF front end electronics system has 432 channels and is designed to run at the 7.58 MHz bunch crossing rate in CDF. The electronics contributes less than 25 ps to the anticipated TOF timing resolution of 100 ps, which is dominated by photon statistics. This paper describes the design and implementation of the electronics as well as the initial in situ performance.**

Keywords— **Time-of-Flight, CDF, Photomultiplier, Scintillator.**

I. Introduction

The CDF Time-of-Flight detector (TOF)[1][2] consists of 216 bars of $4\times4\times279$ cm Bicron BC-408 scintillator located at a radius of 138 cm from the beam line in 4.7 cm of radial space between the Central Outer Tracker and the cryostat for the superconducting solenoid. A Hamamatsu R7761 nineteen-stage fine-mesh photomultiplier tube (PMT) is attached to each end of every bar. The tube can operate in the 1.4T magnetic field of the CDF solenoid with an average gain reduction factor of 500 from the nominal gain of 10^6. For each phototube we measure the pulse arrival time and charge. The expected time-of-flight resolution of our system is 100 ps, which is dominated by photon statistics. Our goal was to build a system in which the electronics contribution to this overall resolution was less than 25 ps.

II. The Electronics Design

A. The Signal Path

Figures 1 and 2 show the signal path and the timing diagram for a single phototube channel. A custom designed high voltage base is attached to the PMT which forms a differential signal from the anode and the last dynode stage. A minimum ionizing particle (MIP) passing through 4 cm of scintillator at the face of the phototube yields a differential signal of about 100 mV when the anode and dynode are terminated into 50Ω and PMT high voltage is set to the expected operating gain. The differential signal is then fed into a preamplifier that drives the signal through a 12 m custom twisted pair signal cable to the TOF transition board, which is the readout front end electronics.

The TOF transition board consists of a 9U high 160 mm wide main transition board (TOMAIN) and three analog daughter boards (TOAD), each of which processes three phototube channels. The PMT signal cable is connected to the TOAD, which contains the analog electronics for pulse shaping, baseline restoration, discrimination, gate generation, time to amplitude conversion (TAC), calibration, and charge measurement. The TOMAIN distributes power and provides programmable voltages, clock fanout, and remote monitoring functions. The charge output is read by a CDF CAFE daughter card [3] that has a 10-bit ADC. The TAC output voltage is digitized by a TOF specific DECAF card with a 12-bit ADC. The final TOF data enters the CDF data stream via the existing ADMEM interface board [3].

Department of Physics and Astronomy, University of Pennsylvania, Philadelphia, PA 19104-6396

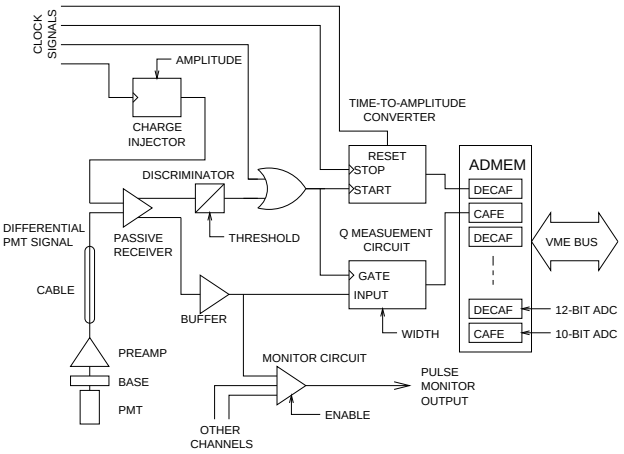

Fig. 1. The block diagram of the electronics processing chain for the signal of one phototube. Most of the signals indicated by a single line for clarity are actually differential signals.

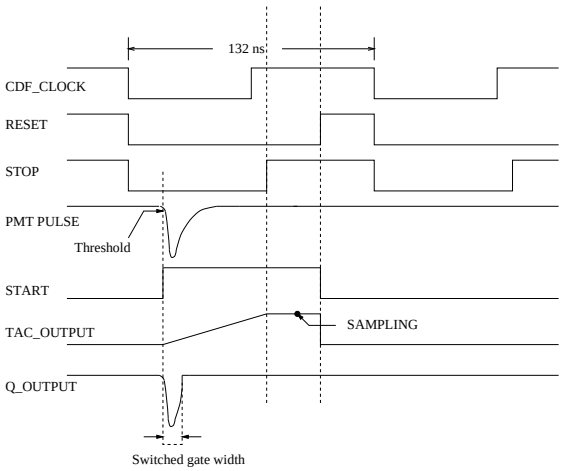

Fig. 2. The timing diagram of the electronics processing chain for the signal of one phototube.

B. The Preamplifier

The preamplifier is mounted directly behind the PMT base and connects to both the anode and last dynode. This technique provides a nearly differential input that helps eliminate common mode pickup to increase the signal to noise ratio. An conceptual schematic diagram of the preamplifier is shown in Fig. 3. The preamplifier consists of two differential amplifier stages and is designed to have a bilinear gain: the gain for a low input signal (a few MIP's) is typically 15 and the gain for a large input signal is typically 2. This bilinear gain is achieved by using a resistor and a shunt diode across the output of the first stage. High bandwidth transistors are used in the two low gain stages to preserve the rise time of the PMT signal. The output is formed using the emitter and collector signal from a gain 1 NPN and PNP transistor driver pair. A balanced zero-offset output is achieved by capacitively cross-coupling the emitter and collector signals from the NPN and PNP output transistors.

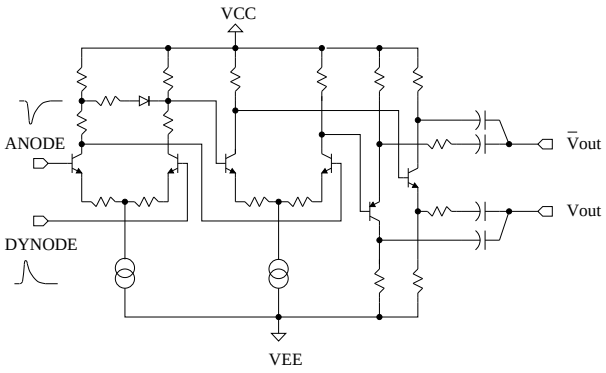

Fig. 3. A conceptual schematic of the TOF preamplifier.

C. Receiver and Discriminator

The differential output signal of the preamplifier propagates over a 12 m shielded twisted pair cable to the TOAD board where an RF transformer provides a balanced signal transfer from the cable to the TOAD board as shown in Fig. 4. A very efficient use of the signal current from the PMT is provided by the termination network. The cable impedance is matched by a parallel network that splits the signal into two paths. One branch utilizes a capacitor and resistor, connected in series, to differentiate the signal, providing the discriminator with good leading edge timing as well as fast settling time to the baseline. The other path is formed by an inductor and resistor in series and provides a bandwidth limited version of the PMT signal to the integrator. Current through the inductor in this branch is delayed and allows time for the discriminator to open the charge integration gate. The imaginary components of the complex impedance are made to cancel by making the time constants in the two branches the same. DC currents in PMT cable are avoided by using a high frequency isolation transformer on the TOAD board.

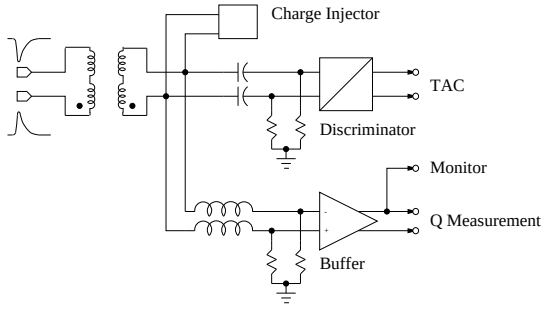

Fig. 4. A conceptual schematic of the Receiver and Discriminator.

D. Time Measurement Circuit

The front-end electronics for the TOF detector is required to provide precise timing information and charge measurement. We desire a timing stability in the electronics better than 25 ps so that photon statistics remains the dominant factor limiting the resolution of a single PMT. This level of timing stability is an order of magnitude beyond what is required for most other CDF II electronics.

The time measurement is made by using a common stop time to amplitude converter. A schematic of the design is shown in Fig. 5. The TAC is intended to have a minimal sensitivity to noise pick up and leakage current on the timing capacitors. The differential ECL START signal from discriminator initiates a linear charging on one of the timing capacitors. The TAC is stopped by a common differential ECL STOP signal produced by a precision clock fanout system. The voltage difference between the two capacitors is then proportional to time. Any change in voltage due to leakage cancels to first order. In addition, any noise present would be picked up equally on both capacitors and would cancel in the difference.

A single ended voltage output of the TAC is generated using a high speed instrumentation amplifier (MAX4145) with the gain of 2. This voltage is digitized on the DECAF card, which has a 12-bit, 25 MSPS ADC (AD9225).

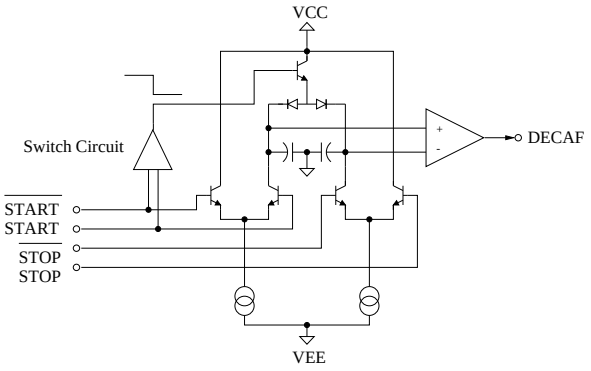

Fig. 5. A conceptual schematic of the time measurement circuit.

E. Charge Measurement Circuit

The primary purpose of the charge measurement circuit is to correct the time measurement for pulse height dependence. The charge measurement can also be used to provide a trigger for highly ionizing particles (e.g. magnetic monopoles). A conceptual schematic is shown in Fig. 6. It is a voltage to current converter with a single ended output that drives current to the CAFE card for charge integration. The CAFE card integrates the current for 132 ns with 1300 pC (10 mA for 132 ns) full scale. In order to avoid including the charge from late photons or a second particle, a gate forces the output of the charge measurement circuit to be zero until it is initialized again by the TAC START. The gate then opens and closes again after an adjustable time delay. The gate width can be set from zero up to 60 ns through an 8-bit DAC on the TOMAIN board.

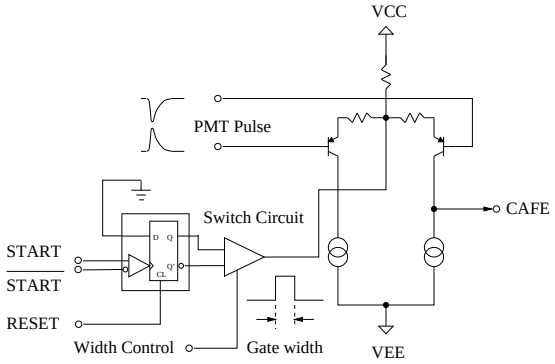

Fig. 6. A conceptual schematic of the voltage to current converter circuit used for the charge measurement.

F. Calibration

Because of the stringent timing requirements for the electronics, variation over time due to temperature drifts, ground voltage shifts or aging of the components must be anticipated. It is essential to include ways of measuring these effects in the design of the electronics.

The electronics calibration is performed using a digital delay generator to provide a differential ECL pulse that is fanned out to selected sets of channels. This signal is used to start the TAC, bypassing the discriminator. The response of the TAC to known delays is measured by stepping through a series of delays with respect to the common stop signal. A second mode of calibration uses the same ECL pulse to trigger a charge injector to send a differential square pulse into the receiver stage for diagnostics and testing, as shown in Fig. 7. The current induced through the transformer is balanced by a matched pair of NPN and PNP transistors to keep the DC bias in the receiver stage unchanged, as well as to minimize interference and noise pickup. The injected charge amplitude is controlled by an 8-bit DAC on the TOMAIN board and its relative phase and width with respect to the STOP signal can be adjusted by the DDG.

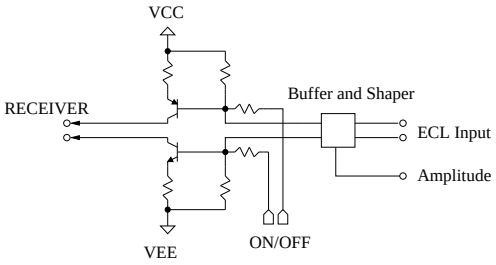

Fig. 7. A conceptual schematic of the charge injector circuit.

G. Remote Monitoring

To facilitate debugging and commissioning of the TOF system, the electronics includes a means of monitoring remotely individual PMT signals (or sums of these signals) as well as the clock signals. The monitor circuit for the PMT signals, as shown in Fig. 8, is a common base current summation circuit. It is turned off by reverse biasing the NPN transistor. The diode network sets the DC bias point of the NPN transistor base and also provides an alternative signal path. The parallel capacitor makes the diode network have a small AC impedance so that the voltage swing at the NPN transistor is small enough, so that even large PMT signal will not change the bias polarity of the NPN transistor while it is off. The monitor circuits of nine channels in the TOF transition board share one common emitter output buffer. The buffer itself is connected to a coaxial RG-58 cable installed on the CDF detector, which gives us the ability to monitor single or multiple channels at any time. ECL clock signals are monitored using differential pair amplifiers with collectors on one leg connected together to drive a 50 Ω cable.

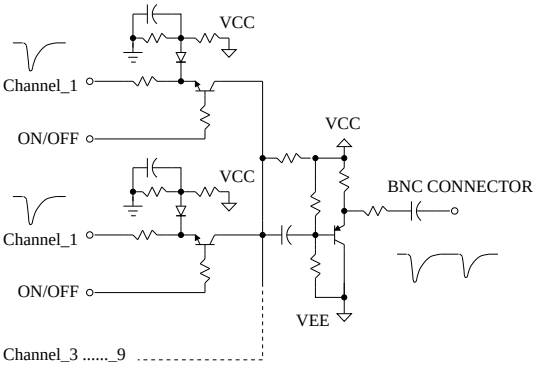

Fig. 8. A conceptual schematic of the PMT pulse monitor circuit.

III. Test Performance

A. Timing Performance

We have performed various studies to determine the intrinsic timing resolution of the system due to the electronics. These studies have been performed with the production electronics mounted on the CDF detector. The values quoted represent the resolution due to all components of

the Time-of-Flight electronics including the clock fanout system which distributes the calibration and common stop signals to all boards mounted on the detector.

The resolution has been studied primarily by examining the widths of the distribution of TAC values with a constant delay inserted between the calibration pulse and common stop inputs. A fixed delay of 40 ns, implemented with a delay cable, consistently yields a resolution of 8.5 ps with long term drifts observed to be less than 9 ps over 40 hours. However, this test does not necessarily represent the resolution that would be obtained for normal operation for which there would a more random arrival time of start signals to the TAC. Using a digital delay generator (Berkeley Nucleonics model B951) with a low frequency external trigger, the timing resolution obtained is typically 25 ps. However, this number includes the intrinsic jitter in the DDG which the manufacturer quotes only as being less than 25 ps and which we have not measured independently.

An important consideration for the use of the electronics for physics analysis is the ability to accurately determine the time which corresponds to a particular value read out from the TAC. Specifically, we find that the residuals from a linear fit to the TAC output as a function of the DDG delay can be as large as 51 ps. However, these residuals can be kept well under 17 ps with an RMS of 4.9 ps by fitting to a non-linear response function:

$$V_{\mathrm{TAC}} = \beta(1 + \gamma e^{-t/\tau}) \cdot t \qquad (1)$$

where β, γ and τ parameters that are determined separately for each channel.

B. Charge Measurement Performance

The response of the charge signal path has been studied in the lab and with the complete system installed in the CDF detector. The response of the ADC to a range of input pulse amplitudes was studied using a PMT exposed to pulses of 430 nm light produced using a solid state infrared laser with a frequency doubling crystal. The ADC response as a function of the PMT gain is shown in Fig. 9 for two different gate width settings.

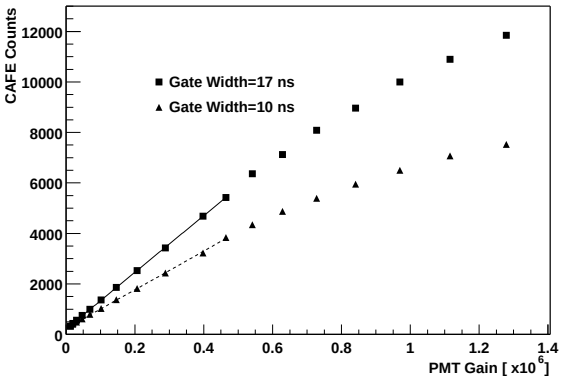

Fig. 9. The CAFE ADC readout *vs.* PMT gain.

Figure 10 shows a peak of the ADC response due to tracks recorded with the CDF detector, which travels the full thickness of the scintillator. The ADC response is scaled by the path length in the scintillator. The scintillator thickness is 4 cm so the typical ADC response to a MIP is of order 1000 counts. The data used to generate this distribution was recorded with the PMT's operated at a gain of 3×10^4 in the magnetic field with a gate width of 17 ns. Hence, with this set of operating conditions, a dynamic range of approximately 12 MIP's can be achieved, albeit with a non-linear response curve, due primarily to the preamplifier's bilinear gain characteristics.

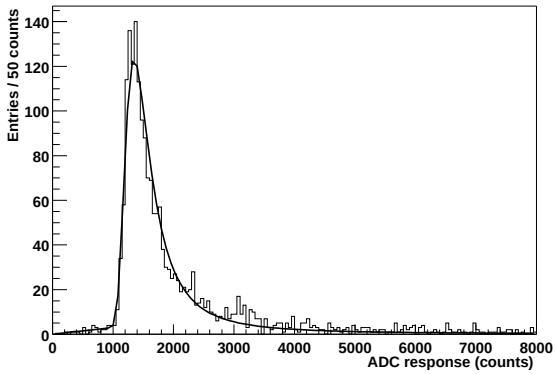

Fig. 10. Distribution of ADC response corrected for path length in the scintillator.

IV. Conclusions

The front end electronics for the TOF were completely installed on the CDF-II detector by August 2001, and the TOF has been included in the CDF-II data stream since that time. Systematic studies of the electronics in test stands and in situ on the experiment have confirmed that the performance of the electronics meets or exceeds the design specifications.

Acknowledgments

The authors would like to acknowledge their colleagues in the Time-of-Flight group for their suggestions and support. We thank C. Alexander, A. Morton, R. Pearce, and M. Scherzer for their help in assembling and testing the electronics.

References

[1] C. Paus et al., "Design and Performance Tests of the CDF Time-of-Flight System," *Nucl. Instrum. Meth.*, vol. A461, pp. 579–581, 2001.

[2] C. Grozis et al., "The Time of Flight Detector at CDF," *Nucl. Phys. Proc. Suppl.*, vol. 93, pp. 344–347, 2001.

[3] Theresa Shaw, Charles Nelson, and Thomas Wesson, "The Design of the CDF Run 2 Calorimetry Readout Module," *IEEE Trans. Nucl. Sci.*, vol. 47, pp. 1834–1838, 2000.